RESEARCH ARTICLE

Design and characterization of a 10 nm finfet

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Abstract

This paper presents the design, characterization, and analysis of a 10 nm silicon negative channel FinFET. To validate the design, we have simulated the output characteristics and transfer characteristics of the transistor. Both of which comply with the standard characteristics of an operational MOSFET. Owing to its efficacy in suppressing short channel effects, the leakage current of the tri-gate transistor is found to be low; whereas, the drive current is sufficiently high. We have also presented the design specifications of the transistor.

Keywords: Drive current, feature size, FinFET, leakage current, saturation current

INTRODUCTION

As VLSI technology advances, the feature length of a MOSFET is being pushed towards nanometric dimensions (Snider & William 2007; Ho *et al.,* 2016). Over the years, the size of a transistor has undergone dramatic reduction. In the 1960s, the feature size of a typical transistor was about 50 μm (Ahmad *et al*., 2006; Yeap *et al*., 2015; Yeap & Nisar, 2018) but today, the size of which could be as small as 15 nm. As the technology node continues to reduce towards the sub-nanometer range, short channel effects and leakage current has become major problems to be overcome by integrated circuit (IC) chip manufacturers. In order to curb with these effects and to enhance the performance of the transistors, Intel Corporation introduced the 22 nm tri-gate transistor or better known as the fin field-effect-transistor (FinFET) in 2011. In comparison with its planar 2D counterpart, the new 3D transistor has better control of the current flow – it reduces current leakage when the transistor is at its "off-state" and minimizes short channel effects at its "on state" (Yeap & Nisar 2018).

Although research reports on FinFETs can be widely found in the literature (Somra *et al.*, 2015; Yu *et al*., 2002; Frank *et al.*, 2001; Bhole *et al.,* 2013), the specifications of the design are surprisingly rare. Here, we present the design specifications and characterization of a 10 nm n-channel FinFET. To verify the design, we simulate the output and transfer characteristics using the three-dimensional Drift-diffusion Charge Control or 3D-DDCC solver and compare the results with those of a standard operational MOSFET.

Design of the 10 nm finfet

The design of our FinFET was based on one of the SOI tri-gate MOSFETs structures as reported in Shehata *et al.,* (2015). This structure is chosen mainly because the gate is able to exert a more thorough control on the channel. This results in lower Drain Induced Barrier Lowering (DIBL) effect. In comparison with the other five

structures in Shehata *et al.,* (2015), it can also be seen that the structure below the gate of the SOI tri-gate is planarized and is therefore, relatively easier to be fabricated. To minimize leakage and to avoid latch-up, we deposited a layer of buried oxide in the substrate. The structure of our design was drawn using the 3D-DDCC solver as shown in Fig. 1. As can be seen from the figure, the structure of the 3D transistor is very much different from its 2D counterpart. Unlike the planar MOSFET, the source and drain terminals of the FinFET protrude out from the substrate surface, resembling closely the fin of a fish. Since the gate encapsulates the inversion layer, the effective width of the transistor is equivalent to the addition of the width and the heights at the two sides of the gate (or drains/source terminal). This feature provides higher current flow in between the source and drain terminals.
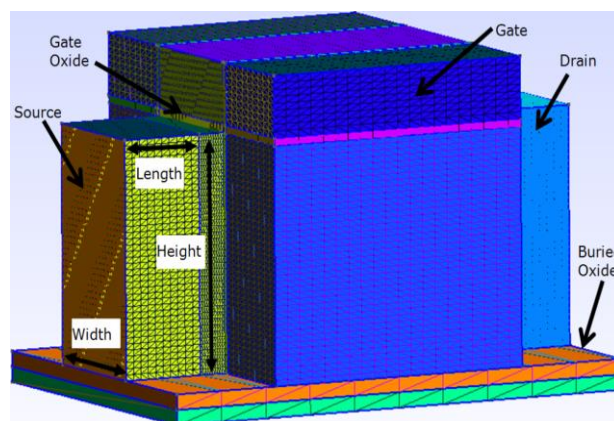

Fig. 1 The geometrical structure and of a FinFET.

RESULTS AND DISCUSSION

The parameters of the n-FinFET are summarized in Table 1. It can be seen from the table that the effective width (i.e. the addition of the width and the two heights of the source or drain terminal in the table) of the transistor is equivalent to 20.5 nm. In the design of the transistor, the dopant densities were carefully adjusted in order to obtain the characteristics of an operational MOSFET.

To validate the design, we connected the gate and drain terminals to voltage supply V_G and V_D, respectively. Both source and substrate terminals were grounded. To obtain the output current-voltage (IV) characteristics, we fixed V_G at different values and vary V_D. The corresponding drain current I_D values were then simulated. Fig. 2 to 4 depict the output characteristics at $V_G = 1.0$ V to 3.0 V. Upon close inspection on the figures, it can be observed that the current curves go through both linear and saturation phases. Although the I_D currents presented here are found to be relatively higher, they are considered close to the measurement results in Yu *et al.*, (2002). The difference in performance can be attributed to the different specifications (the dopant concentration, activation energy, etc.) used in both designs. It is apparent that our design allows higher current I_D flow when the drain voltage V_D is held constant. Table 2 summarizes the saturation points at different V_G. It can be seen that the saturation voltages and currents increase as V_G increases. The characteristic curves therefore comply with those of an operational enhancement mode MOSFET (Sze 2002). It is worth noting that when the feature size shrinks below the submicron regimes, channel length modulation becomes apparent. Hence, instead of being constant, currents beyond the saturation points are found to be increasing.

In order to produce the transfer characteristic curves, we fixed V_D at different values and simulate I_D at a range of V_G. Fig. 5 to 8 illustrate I_D as a function of V_G at $V_D = 0$ V to 3 V. The leakage and drive currents found from the figures are summarized in Table 3. As can be seen from the table, the leakage or sub-threshold currents (i.e. the drain current at the sub-threshold region) are low and is almost negligible at $V_D = 0$ V; whereas the drive currents are sufficiently high, particularly at $V_D = 3.0$ V. We attributed the low leakage current to the layer of buried oxide deposited between the transistor and substrate. Since our transistor was fabricated on the Silicon-on-Insulator (SOI) substrate, the buried oxide deposited exactly below the drain was effective in suppressing the increase of the depletion region at the drain-substrate interface. The DIBL short-channel effect which is caused by the excessive increase of the depletion region can therefore be avoided. In other words, the sub-threshold swing of the transistor can also be significantly improved. Since the gate structure encapsulates the inversion layer, it also provides effective control on the electron flow between the source and drain terminals, resulting in high drive current.
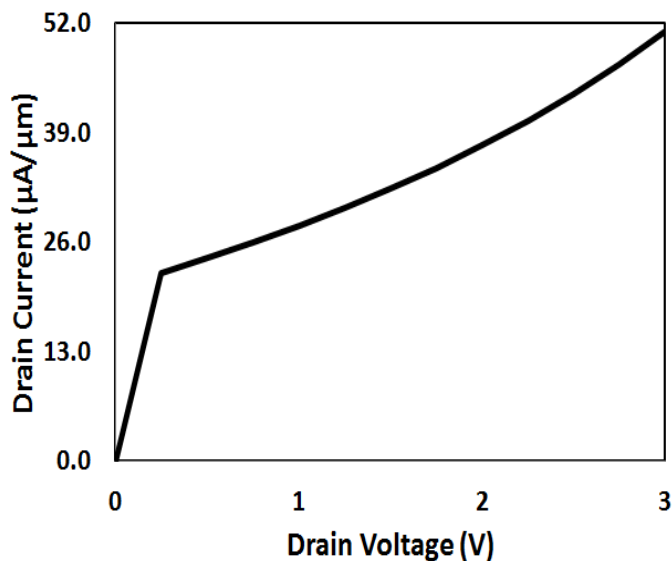

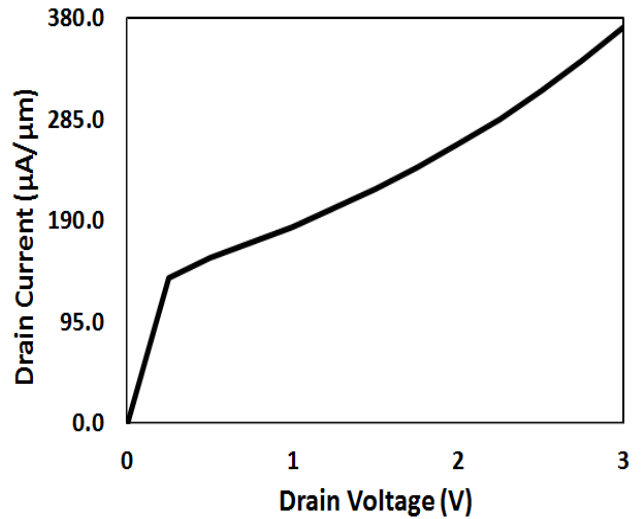**Fig. 3** I-V characteristics of n-FinFET at $V_G = 2$ V.

Fig. 4 I-V characteristics of n-FinFET at $V_G = 3$ V.
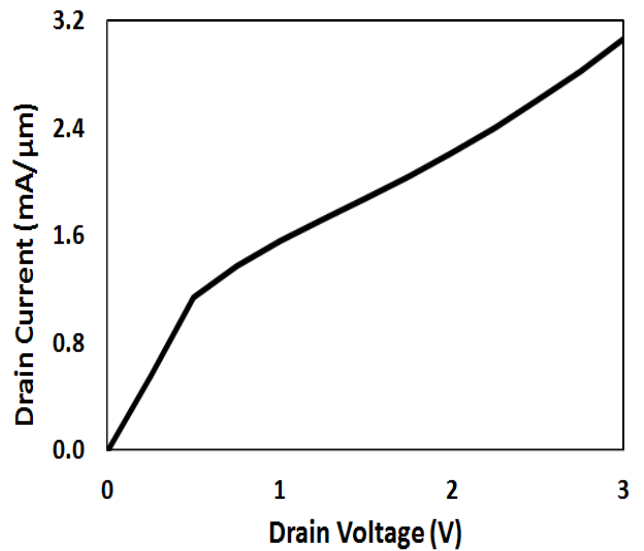

Fig. 2 I-V characteristics of n-FinFET at $V_G = 1$ V.
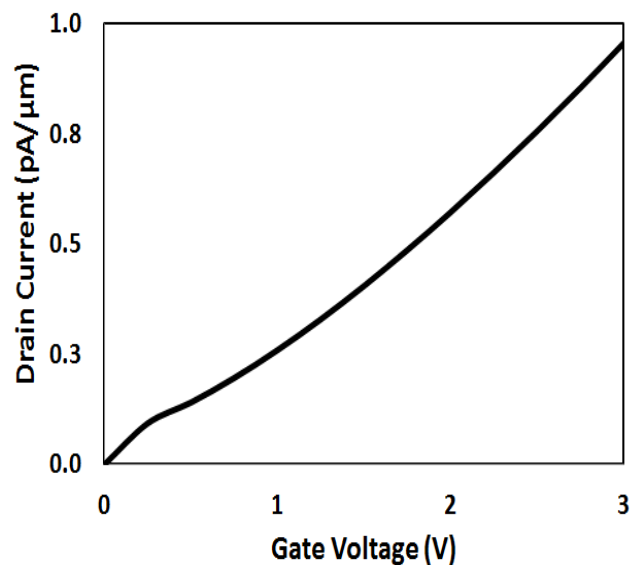

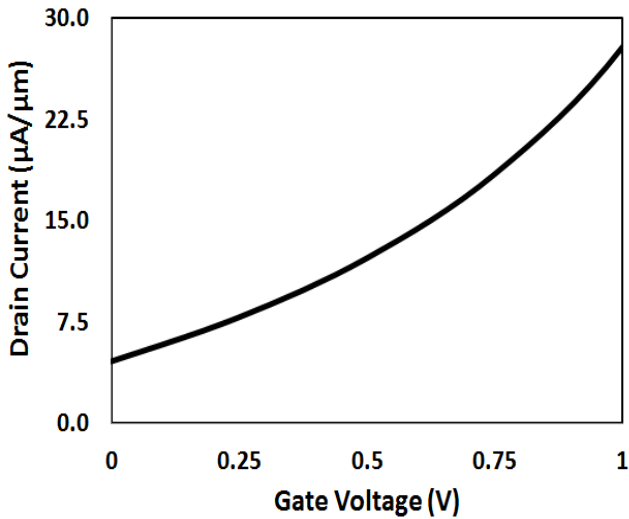**Fig. 5** Transfer characteristics of n-FinFET at $V_D = 0$ V.

Fig. 6 Transfer characteristics of n-FinFET at $V_D = 1$ V.
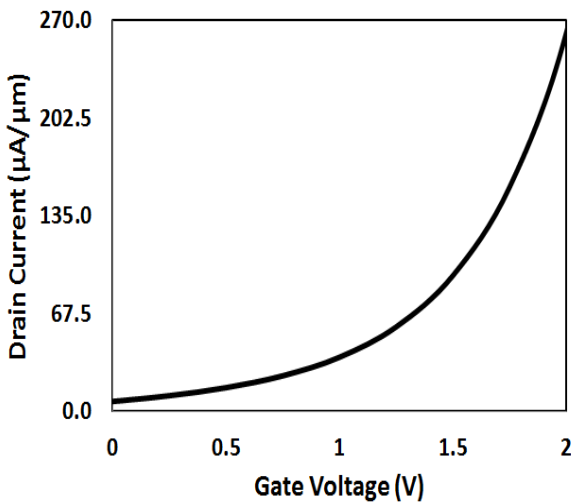

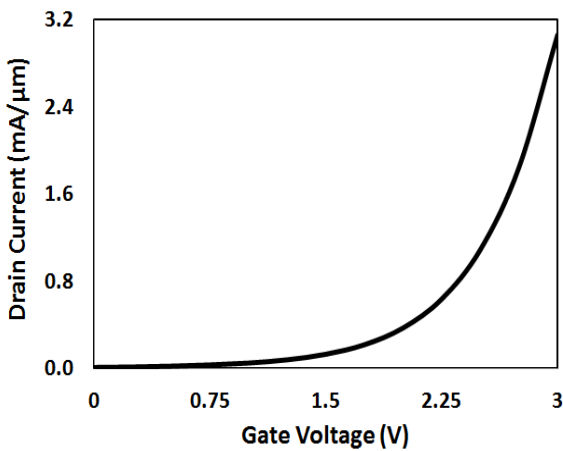**Fig. 7** Transfer characteristics of n-FinFET at $V_D = 2$ V.

Fig. 8 Transfer characteristics of n-FinFET at $V_D = 3$ V.

Table 1 Parameters of the 10 nm n-FinFET.

Region	Parameters	
Drain	Dopant concentration:	$1.0 \times 10^{18}\ cm^{-3}$
	Activation energy:	0.025 eV
	Length:	3 nm
	Width:	5 nm
	Height:	7.75 nm
Source	Dopant concentration:	$1.0 \times 10^{18}\ cm^{-3}$
	Activation energy:	0.025 eV
	Length:	3 nm
	Width:	5 nm
	Height:	7.75 nm
Buried Oxide	Activation energy:	0.025 eV
	Length:	18 nm
	Thickness:	1 nm
Gate Oxide	Length:	10 nm
	Thickness:	0.25 nm
Substrate	Activation energy:	0.025 eV
	Dopant concentration:	$1.0 \times 10^{15}\ cm^{-3}$
	Length:	18 nm
	Thickness:	4 nm

Table 2 Saturation points of the 10 nm n-FinFET.

Gate voltage, V_G (V)	Saturated current, $I_{D,SAT}$ (µA/µm)	Saturated voltage, $V_{D,SAT}$ (V)
1	22.4	0.25
2	136.9	0.25
3	1136.4	0.5

Table 3 On and off currents of the10 nm n-FinFET.

Drain voltage, V_D (V)	Drive current, I_{DRIVE} (µA/µm)	Leakage Current, I_{OFF} (µA/µm)
0	0	0
1	27.9	4.6
2	261.7	7.0
3	3062.9	9.8

CONCLUSION

We have designed and analyzed the performance of a 10 nm n-channel silicon FinFET. The design was verified by comparing its output characteristics with those of an operational transistor. The transfer characteristic curves showed that the transistor has low leakage current and sufficiently high drive current. As the technology node continues to shrink, it can be foreseen that FinFETs will gradually replace planar MOSFETs as the fundamental building block of integrated circuits. Since the 3D transistor is becoming more and more prevalent, it may be worthwhile looking into the issue of field accumulation at the corners of the gate structure. More commonly known as the "corner effect", the accumulation of electric field at the corner regions may result in higher sub-threshold swing and threshold voltage. The increase in both of these is undesirable and should therefore be avoided.

ACKNOWLEDGEMENT

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